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10/678,672	10/02/2003	Robert C. Chang	SANDP034	9759

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EXAMINER	
GOGIA, ANKUR	

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,672	CHANG ET AL.	
	Examiner	Art Unit	
	Ankur Gogia	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application, having Application No. 10/678,672, has a total of 28 claims pending in the application; there are 2 independent claims and 26 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Priority

3. The examiner acknowledges claim for priority based on U.S. Provisional Patent Application No. 60/421,910, filed 28 October 2002.

Drawings

4. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

5. As required by M.P.E.P. 609(c), the applicant's submission of the Information Disclosure Statement dated 27 October 2003 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P. 609(c)(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

Specification

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

7. Claim 17 is objected to because of the following informalities: The claim discloses wherein the memory area is one of a third physical block and a RAM cache. The claim appears to be disclosing the memory area as either a third physical block or a RAM cache and therefore more appropriate language would be "one of a third physical block **or** a RAM cache". Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 10-14 and 19-28 are rejected under 35 U.S.C. 112, first paragraph, as failing to meet the written description requirement.

10. Claim 10 discloses writing the first and third updates to the memory area upon determining that there is no other set of contents to be obtained. However the specification discloses writing the updates to the memory area as they are obtained and writing them to the second physical block upon determining that there are no more set of contents to be obtained **(Fig. 5)**. The specification does not appear to mention the embodiment disclosed in claim 10 and therefore the written description requirement does not appear to be met.

11. Claims 11-14 are rejected for inheriting the deficiencies of the claim(s) from which they depend.

12. Claim 19 discloses, "storing the contents of the cache into the **second physical block**" on Pg. 48, Line 6. However, on lines 8-9 the claim discloses "wherein storing the contents of the cache includes storing the first update into a first physical group in the **first physical block**". The specification discloses that updates are stored in cache and the cache is then stored into a second physical block only **(Figs. 5 and 9)**. The specification does not appear to disclose wherein the contents of the cache are stored in the second physical block along with the update being stored into the first physical block. Therefore the written description requirement does not appear to be met.

13. Claims 20-28 are rejected for inheriting the deficiencies of the claim(s) from which they depend.

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claims 1-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

16. The term "substantially" in claim 1 is a relative term which renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not appear to provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The examiner cannot determine as to what degree a logical block has to be mapped to a physical block for the logical block to be "substantially mapped" to the physical block. For the instant Office Action, the examiner interprets "substantially mapped" as fully mapped.

17. The term "substantially" in claims 3 and 14 is a relative term which renders the claims indefinite. The term "substantially" is not defined by the claims, the specification does not appear to provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The examiner cannot determine as to what degree a logical block has to be unmapped from a physical block for the logical block to be "substantially unmapped" from the

physical block. For the instant Office Action, the examiner interprets "substantially unmapped" as being fully unmapped.

18. Claim 9 states on line 11, "obtaining a third set of contents, the **first** set of contents being associated with a second logical group..." however claim 1, which claim 9 depends from, discloses that the first set of contents is associated with a first logical group. It is believed that the applicant intended to state in claim 9, "obtaining a third set of contents, the **third** set of contents...". For the instant office action, the examiner interprets the claim as "the **third** set of contents...". Appropriate correction is required.

19. Claim 10 discloses that the first and third set of contents is written into the memory area when there is no other set of contents associated with the first logical block to be obtained. However, the first set of contents has already been written to the memory area as disclosed in claim 1 and the third set of contents have already been written to the memory area as disclosed in claim 9. The examiner cannot determine whether the first and third set of contents are being rewritten to the memory area or the applicant intended to further limit claims 1 and 9 such that when the writing is performed when it is determined that no other set of contents is to be obtained or if the first and third contents are to be written to the second physical block upon determining that no other set of contents is to be obtained. For the instant Office Action, the examiner interprets the claim as the third option, as this is the only option that appears to be supported by the specification. Appropriate correction is required.

20. The term "substantially" in claims 10 and 11 is a relative term which renders the claims indefinite. The term "substantially" is not defined by the claims, the specification

does not appear to provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The examiner cannot determine as to what range of values defines "substantially no" other set of contents to be obtained and for the instant Office Action, the examiner interprets that zero set of contents to be obtained is "substantially no" set of contents to be obtained.

21. The term "substantially" in claim 12 is a relative term which renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not appear to provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The examiner cannot determine as to how immediately "substantially immediately" is. Since the art is related to the computer art, where time is measured in various degrees of magnitudes of seconds, substantially immediately could be interpreted over a large range. For the instant office action, the examiner interprets "substantially immediately" as meaning the event is triggered to occur after a certain preceding event has completed.

22. The term "substantially" in claim 23 is a relative term which renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not appear to provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The examiner cannot determine as to when a portion of the copied contents has been

"substantially overwritten". For the instant Office Action, the examiner interprets "substantially overwritten" to be when all necessary items have been overwritten.

23. Claim 19 discloses, "storing the contents of the cache into the **second physical block**" on Pg. 48, Line 6. However, on lines 8-9 the claim discloses "wherein storing the contents of the cache includes storing the first update into a first physical group in the **first physical block**". From these limitations it cannot be determined whether the contents of the cache are stored in the second physical block along with the update being stored in the first physical block, in which case the update would be stored in the first and second physical blocks. Based on the disclosure in the specification **(Figs. 5 and 7)** it appears that the updates are stored in cache and then moved to the second physical block only and the examiner has interpreted the claim as such for the instant Office Action.

24. Any claim rejected in ¶15 and not specifically addressed above, is rejected for inheriting the deficiencies of the claim(s) from which it depends.

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 1-17, 19-27 are rejected under 35 U.S.C. 103(a) as being obvious over applicant's admitted prior art (hereinafter referred to as AAPA) in view of Hagiwara et al.

(2003/0110343; hereinafter referred to as Hagiwara) and "A Space-Efficient Flash Translation Layer for CompactFlash Systems" (hereinafter referred to as NPL) with NPL being provided for extrinsic evidence..

(Note: Hagiwara contains certain figures labeled as #a and #b (i.e. 12a and 12b). In the discussions to follow references to a set of such figures will be made with just the # (i.e. 12a and 12b as a set will be referred to as 12))

Independent Claim 1

AAPA discloses a method for processing contents associated with blocks of a non-volatile memory **(Pg. 2, Line 10, flash memory chip)**, the non-volatile memory being associated with a memory system **(Pg. 2, Line 7)**, the method comprising:

Obtaining a first set of contents **(Fig. 1.204c; Pg. 2, Lines 24-26, new data)**, the first set of contents being associated with a first logical group **(inherent; As shown in NPL on page 367 Sec. II Background ¶2, flash memory is divided into blocks consisting of multiple pages)** of the first logical block **(Fig. 1.202; Pg. 2, Line 25)**, the first group including a first plurality of logical pages associated with the first logical block **(inherent; As shown in NPL on page 367 Sec. II Background ¶2, flash memory is divided into blocks consisting of multiple pages)**, the first logical block being substantially mapped to a first physical block **(Fig. 1.212; Pg. 2, Lines 26-28)**;

Writing the first set of contents into a first physical group **(inherent; As shown in NPL on page 367 Sec. II Background ¶2, flash memory is divided into blocks consisting of multiple pages)** of a second physical block **(Fig. 1.222; Pg. 2, Lines 26-29)**, the first physical group including a first plurality of physical pages **(inherent; As**

shown in NPL on page 367 Sec. II Background ¶2, flash memory is divided into blocks consisting of multiple pages) associated with the second physical block **(Fig. 2.262; Pg. 2, Line 23 – Pg. 3, Line 3; Note that the reference does not disclose writing the first contents from the memory area into the first physical group of the second physical block, rather it is written directly)**; and

Mapping the second physical block to the first logical block **(Pg. 3, Lines 3-4)**.

AAPA does not disclose expressly writing the first set of contents into a memory area and then writing the first set of contents from the memory area into a first physical group of a second physical block, the first physical group including a first plurality of physical pages associated with the second physical block.

Hagiwara discloses a file system for a flash memory wherein updates to a first physical block **(first set of contents)** are stored in a cache memory **(memory area)** and merged with the un-updated data into a second physical block **(first physical group of a second physical block)** at a predetermined time **(Figs. 12, 14-25; ¶s 123-124)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to incorporate a cache to temporarily store updates to pages of a flash memory.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 1.

Claim 2

AAPA further discloses wherein the first physical block includes a second set of contents **(Fig. 1.214a-214f; Pg. 2, Line 29 – Pg. 3, Line 2; all physical pages except the physical page corresponding to an updated logical page)** and the method further including

Writing at least some of the second set of contents into the second physical block with the first set of contents **(Fig. 2.262; Pg. 2, Line 29 – Pg. 3, Line 2)**.

Claim 3

AAPA further discloses erasing the second set of contents from the first physical block; **(Fig. 2.266; Pg. 4, Lines 10-14)** and

Substantially unmapping the first physical block from the first logical block **(Fig. 2.270; Pg. 4, Lines 10-14)**.

Claim 4

AAPA discloses the method of claim 3 as above.

AAPA does not disclose expressly erasing the first set of contents from the memory area.

Hagiwara discloses clearing updates from the cache once they are merged into a physical block **(Fig. 15.S1314)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to erase temporarily stored updates from a cache once the updates were moved to the physical block.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 4.

Claim 5

AAPA discloses wherein the first physical block includes a second set of contents **(Fig. 1.214a-214f; Pg. 2, Line 29 – Pg. 3, Line 2, all physical pages except the physical page corresponding to an updated logical page)**.

AAPA does not disclose expressly writing the second set of contents into the memory area.

Hagiwara discloses when a bank is to be updated, writing the entire bank to the cache **(Fig. 12b.S1012)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to copy a bank to be updated to a cache memory.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 5.

Claim 6

AAPA discloses method of claim 5 as above.

AAPA does not disclose expressly wherein writing the first set of contents into the memory area includes overwriting at least some of the second set of contents in the memory area.

Hagiwara discloses overwriting at least some of the second set of contents in the memory area **(Fig. 12b.S1014; In step S1014 which precedes S1014 an entire bank is copied to the cache and the necessary file blocks are updated within the cache in step S1014)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to update blocks of a physical page in cache.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 6.

Claim 7

AAPA discloses the method of claim 6 as above.

AAPA does not disclose expressly wherein the memory area is a RAM cache.

Hagiwara discloses wherein the memory area is a RAM cache **(Fig. 8.3100)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to use a RAM cache as a cache.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 7.

Claim 8

AAPA further discloses wherein the first set of contents includes an update associated with the first logical block **(Pg. 2, Lines 24-26, new data)**.

Claim 9

AAPA and Hagiwara disclose the method of claim 1 as above.

AAPA further discloses obtaining a third set of contents **(Fig. 1.204a'; Pg. 3, Lines 8-10)**, the first set of contents **(Interpreted as the third set of contents as per discussion in ¶9 above)** being associated with a second logical group **(inherent; As shown in NPL on page 367 Sec. II Background ¶2, flash memory is divided into**

blocks consisting of multiple pages) of the first logical block **(Fig. 1.202'; Pg. 3, Lines 8-10)**, the second logical group including a second plurality of logical pages associated with the first logical block **(inherent; As shown in NPL on page 367 Sec. II Background ¶2, flash memory is divided into blocks consisting of multiple pages)**. AAPA further discloses writing the third set of contents into a third physical block **(Fig. 1.232)** and not the memory area or second physical block.

AAPA does not disclose expressly writing the third set of contents into the memory area; and writing the third set of contents into a second physical group of the second physical block, the second physical group including a second plurality of physical pages associated with the second physical block.

Hagiwara discloses a file system for a flash memory wherein updates to a first physical block **(third set of contents)** are stored in a cache memory **(memory area)** and merged with the un-updated data into a second physical block **(second physical group of a second physical block)** at a predetermined time **(Figs. 12, 14-25; ¶s 123-124)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to incorporate a cache to temporarily store updates to pages of a flash memory.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 9.

Claim 10

AAPA and Hagiwara disclose the method of claim 9 as above.

AAPA does not disclose expressly determining when there is substantially no other set of contents associated with the first logical block to be obtained, wherein when it is determined that there is substantially no other set of contents to be obtained, the first set of contents and the third set of contents are written into the memory area.

Hagiwara discloses writing the contents of the cache to the physical block upon the cache being full **(Fig. 12b.S1008,S1010; When the cache is full the system can no longer process updates and therefore must clear the cache to process more updates)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to clear the memory area when there are no more updates to process.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 10.

Claim 11

AAPA and Hagiwara disclose the method of claim 10 as above.

AAPA does not disclose expressly wherein determining when there is substantially no other set of contents associated with the first logical block to be obtained includes determining when a second logical block is to be updated.

Hagiwara discloses wherein all file blocks in a bank are processed before another bank is processed **(Fig. 12; As is shown in the figure, a bank is placed in the cache at S1012 and all updates to that bank are processed before any updates to another bank are processed S1006)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to clear the memory area when there are no more updates to process.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 11.

Claim 12

AAPA and Hagiwara disclose the method of claim 10 as above.

AAPA does not disclose expressly wherein when it is determined that the second logical block is to be updated, the method further includes:

Substantially immediately obtaining the second physical block; and

Substantially immediately writing the first set of contents and the third set of contents into the second physical block.

Hagiwara discloses when the cache is full to obtain a second physical block and move the contents of the cache to the second physical block **(Fig. 12b.S1008,S1010)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to obtain a second physical block clear the memory area into the second physical block when there are no more updates to process.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 12.

Claim 13

AAPA and Hagiwara disclose the method of claim 12 as above.

AAPA further discloses wherein obtaining the second physical block includes mapping the second physical block to the first logical block **(Pg. 3, Lines 24-26)**.

Claim 14

AAPA further discloses erasing the second set of contents from the first physical block; **(Fig. 2.266; Pg. 4, Lines 10-14)** and

Substantially unmapping the first physical block from the first logical block **(Fig2.270; Pg. 4, Lines 10-14)**.

Claim 15

AAPA further discloses obtaining the second physical block **(Fig. 2.258; Pg. 3, Lines 24-26)**; and mapping the second physical block to the first logical block **(Pg. 3, Lines 24-26)**.

Claim 16

AAPA further discloses wherein the first physical block is not arranged to accommodate the first set of contents **(Pg. 2, Lines 17-20)**.

Claim 17

AAPA and Hagiwara disclose the method of claim 1 as above.

AAPA does not disclose expressly wherein the memory area is one of a third physical block and a RAM cache.

Hagiwara discloses wherein the memory area is a RAM cache **(Fig. 8.3100)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to use a RAM cache as a cache.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 17.

Independent Claim 19

AAPA discloses a method for processing updated contents associated with a first logical block **(Fig. 1.202; Pg. 2, Line 25)** within a non-volatile memory system **(Pg. 2, Lines 15-21, flash memory system)**, the first logical being mapped to a first physical block **(Fig. 1.212; Pg. 2, Lines 26-28)**, the method comprising:

Receiving a first update **(Fig. 1.204c; Pg. 2, Lines 24-26, new data)** associated with the first logical block, wherein the first update is an update to a first logical group **(inherent; As shown in NPL on page 367 Sec. II Background ¶2, flash memory is divided into blocks consisting of multiple pages)** of the first logical block, the first logical group being arranged to include a first plurality of logical pages associated with the first logical block **(inherent; As shown in NPL on page 367 Sec. II Background ¶2, flash memory is divided into blocks consisting of multiple pages)**; and

Mapping the second physical block to the first logical block after the contents of the cache are stored into the second physical block **(Fig. 2.258; Pg. 3, Lines 24-26)**; and

Unmapping the first physical block from the first logical block after the contents of the cache are stored into the second physical block **(Fig. 2.270; Pg. 4, Lines 10-14)**.

AAPA does not disclose expressly

Storing the first update into a cache;

Determining when to store the contents of the cache into a second physical block, the contents of the cache including the first update;

Storing the contents of the cache into the second physical block when it is determined that the contents of the cache are to be stored into the second physical block, wherein storing the contents of the cache includes storing the first update into a first physical group **(inherent; As shown in NPL on page 367 Sec. II Background ¶2, flash memory is divided into blocks consisting of multiple pages)** in the first physical block, the first physical group including a first plurality of physical pages included in the first physical group **(inherent; As shown in NPL on page 367 Sec. II Background ¶2, flash memory is divided into blocks consisting of multiple pages)**.

Hagiwara discloses a file system for a flash memory wherein updates to a first physical block **(first update)** are stored in a cache memory and upon the cache being full **(determining when to store the contents of the cache into a second physical block)** the contents of the cache, which includes the update, are stored in a second physical block **(first physical group of a second physical block)**. **(Figs. 12, 14-25; ¶s 123-124)**

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to incorporate a cache to temporarily store updates to pages of a flash memory.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 19.

Claim 20

AAPA and Hagiwara disclose the method of claim 19 as above.

AAPA does not disclose expressly wherein determining when to store the contents of the cache into the second physical block includes determining when a second logical block is to be processed, and wherein when it is determined that the second physical block is to be processed, the contents of the cache are stored into the second physical block.

Hagiwara discloses wherein all file blocks in a bank are processed before another bank is processed and moving a new bank to the cache when a block in the bank is to be processed after clearing the cache **(Fig. 12)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to clear the memory area when there are no more updates to process.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 20.

Claim 21

AAPA further discloses obtaining the second physical block **(Fig. 2.258; Pg. 3, Lines 24-26)**.

Claim 22

AAPA and Hagiwara disclose the method of claim 19 as above.

AAPA does not disclose expressly wherein the contents of the cache include at least some contents associated with the first physical block.

Hagiwara discloses when a bank **(first physical block)** is to be updated, writing the entire bank to the cache **(Fig. 12b.S1012)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to copy a bank to be updated to a cache memory.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 22.

Claim 23

AAPA and Hagiwara disclose method of claim 22 as above.

AAPA does not disclose expressly copying contents of the first physical block into the cache, wherein when the first update is stored into the cache, the first update substantially overwrites at least a portion of the copied contents associated with the first physical block.

Hagiwara discloses when a bank **(first physical block)** is to be updated, writing the entire bank to the cache **(Fig. 12b.S1012)** and further discloses overwriting at least some of the second set of contents in the memory area **(Fig. 12b.S1014; In step S1014 which precedes S1014 an entire bank is copied to the cache and the necessary file blocks are updated within the cache in step S1014)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to update blocks of a physical page in cache.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 23.

Claim 24

AAPA discloses the method of claim 23 as above.

AAPA does not disclose expressly wherein the cache is a RAM cache.

Hagiwara discloses wherein the cache is a RAM cache **(Fig. 8.3100)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to use a RAM cache as a cache.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 24.

Claim 25

AAPA and Hagiwara disclose the method of claim 19 as above.

AAPA does not disclose expressly wherein determining when to store the contents of the cache into the second physical block includes determining when a second logical block is to be processed, and wherein when it is determined that the second physical block is to be processed, at least some of the contents of the cache are stored into the second physical block.

Hagiwara discloses wherein all file blocks in a bank are processed before another bank is processed and moving a new bank to the cache when a block in the bank is to be processed after clearing the cache **(Fig. 12)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to clear the memory area when there are no more updates to process.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 25.

Claim 26

AAPA further discloses storing at least some of the contents of the first physical block into the second physical block when it is determined that the second logical block is to be processed **(Fig. 2.262; Pg. 2, Line 29 – Pg. 3, Line 2)**.

Claim 27

AAPA and Hagiwara disclose the method of claim 25 above.

AAPA does not disclose expressly erasing the first physical block after at least some of the contents of the cache are stored into the second physical block.

Hagiwara discloses erasing the first physical block after at least some of the contents of the cache are stored into the second physical block **(Fig. 16b.S1420)**.

AAPA and Hagiwara are analogous art because they are from the same field of endeavor of improving the life span of flash type memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of AAPA and Hagiwara before them, to clear the first physical block when the block has been moved to a new physical block.

The motivation for doing so would have been to reduce the number of bank erasures and thereby increase the life of a flash type memory **(Hagiwara ¶125)**.

Therefore, it would have been obvious to combine Hagiwara with AAPA for the benefit of decreased bank erasures to obtain the invention as specified in claim 27.

27. Claims 18 and 28 are rejected under 35 U.S.C. 103(a) as being obvious over AAPA in view of Hagiwara as applied to claim 1 above, and further in view of "A Space-Efficient Flash Translation Layer for CompactFlash Systems" (hereinafter referred to as NPL).

Claim 18

The combination of AAPA and Hagiwara discloses the method of claim 1 as above.

The combination of AAPA and Hagiwara does not disclose expressly wherein the non-volatile memory is a NAND flash memory.

NPL discloses wherein a NAND flash memory may be implemented in a system for improving performance of a flash memory device **(Page 367, Sec. II Background, ¶s 3-4)**.

The combination of AAPA and Hagiwara and NPL are analogous art because they are from the same field of endeavor of improving performance of flash memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the combination of AAPA and Hagiwara and NPL before them, to use a NAND type flash memory.

The motivation for doing so would have been NAND type flash memories have efficient bulk read/write operations and relatively short erase time **(NPL - Pg. 367, Sec. II Background, ¶4)**.

Therefore, it would have been obvious to combine NPL with the combination of AAPA and Hagiwara for the benefit of efficient bulk read/write operations and relatively short erase time to obtain the invention as specified in claim 18.

Claim 28

The combination of AAPA and Hagiwara discloses the method of claim 25 as above.

The combination of AAPA and Hagiwara does not disclose expressly wherein the cache is a physical block cache.

NPL discloses using a physical block as a cache to store updates **(Pg. 368, Sec. III.A The Log Block)**.

The combination of AAPA and Hagiwara and NPL are analogous art because they are from the same field of endeavor of improving performance of flash memory devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art, having the teachings of the combination of AAPA and Hagiwara and NPL before them, to use a physical block as a cache.

The motivation for doing so would have been to reduce the number of erasures to the memory **(NPL - Pg. 369, Sec. III.B Merge Operation, ¶4)**.

Therefore, it would have been obvious to combine NPL with the combination of AAPA and Hagiwara for the benefit of reduced number of erasures to obtain the invention as specified in claim 28.

Conclusion

28. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. 707.07(i):

a. Per the instant office action, claims 1-28 have received a first action on the merits and are subject of a first action non-final.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ankur Gogia whose telephone number is 571-272-4166. The examiner can normally be reached on M-F 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ankur Gogia
Examiner
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2/2/06

CHRISTIAN CHACE
PRIMARY EXAMINER